WHAT IS CLAIMED IS:

1. A electronic device comprising:

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; and

a switch configured to decouple said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce the parasitic capacitance of said data bus, wherein the switch is an integrated part of the memory circuit.

2. The electronic device of Claim 1 comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

3. The electronic device of Claim 1, wherein the memory circuit comprises a synchronous DRAM memory.

4. A electronic device comprising:

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; and

a switch configured to decouple said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce the parasitic capacitance of said data bus,

wherein the switch, the memory circuit and the memory controller are integrated into a single circuit.

5. The electronic device of Claim 4, additionally comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

6. The electronic device of Claim 4, wherein the memory circuit comprises a synchronous DRAM memory.

7. A electronic device comprising:

a memory controller;

a memory circuit;

a data bus coupling said memory controller and said memory circuit; and

a switch configured to decouple said data bus from said memory circuit when no memory access is being requested by said memory controller so as to reduce the parasitic capacitance of said data bus,

wherein the switch, the memory circuit and the memory controller are integrated into a single circuit.

8. The electronic device of Claim 7, comprising a plurality of memory circuits and a corresponding plurality of decoupling means.

9. The electronic device of Claim 7, wherein the memory circuit comprises a synchronous DRAM memory.

10. A state decoder circuit, comprising:

a state decoder configured to receive an address signal targeted for a memory circuit and having an input coupled to memory control signals and an output, wherein said state decoder is configured to have an output signal having a first state during a memory access and a second state in the absence of a memory access, and wherein the state decoder is configured to activate a switch to decouple a memory circuit from a data bus when no memory access cycle is being performed.

11. The state decoder circuit of Claim 10, wherein the address signal comprises a row address strobe signal.

12. The state decoder circuit of Claim 10, wherein the address signal comprises a column address strobe signal.

13. The state decoder circuit of Claim 10, wherein the state decoder is integrated with a printed circuited circuit board.

14. The state decoder circuit of Claim 13, wherein the printed circuit board is integrated with the memory circuit.

15. The state decoder circuit of Claim 14, wherein the memory circuit comprises synchronous-DRAM memory,

16. A switch, comprising:

a plurality of inputs connected to corresponding ones of first plurality of electrical contacts, and a plurality of outputs connected to at least one memory integrated circuit so as to couple a data bus from said first plurality of electrical contacts to said memory integrated circuit, said at least one switch having an additional input coupled to a state decoder circuit output that is responsive to an address signal, and responsive to said state decoder circuit output to decouple said memory circuit from said data bus when no memory access cycle is being performed.

17. The switch of Claim 16, wherein the switch is integrated with a printed circuit board.

18. The state decoder circuit of Claim 16, wherein the address signal comprises a row address strobe signal.

19. The state decoder circuit of Claim 16, wherein the address signal comprises a column address strobe signal.

20. A electronic device comprising:

a printed circuit board;

a memory controller mounted on said printed circuit board;

a bus switch mounted on said printed circuit board;

a first data bus connecting said memory controller and said bus switch;

a plurality of memory devices including at least a first and a second memory device mounted on said printed circuit board; and

a second data bus connecting said bus switch to said first memory device and a third data bus connecting said bus switch to said second memory device, wherein said bus switch is configured to couple said first data bus to said second data bus during memory accesses directed to said first memory device, and wherein said bus switch is configured to couple said first data bus to said third data bus during memory accesses directed to said second memory device

a state decoder configured to receive an address signal targeted for either the first or second memory device, and wherein the first memory device or second memory device is selectively decoupled from the bus in response to a change in state in the address signal.

21. A printed circuit board;

a memory controller mounted on said printed circuit board;

a bus switch mounted on said printed circuit board;

a first data bus connecting said memory controller and said bus switch;

a plurality of memory devices including at least a first and a second memory device mounted on said printed circuit board;

a second data bus connecting said bus switch to said first memory device and a third data bus connecting said bus switch to said second memory device, wherein said bus switch is configured to couple said first data bus to said second data bus during memory accesses directed to said first memory device, and wherein said bus switch is configured to couple said first data bus to said third data bus during memory accesses directed to said second memory device; and

a state decoder configured to receive an address signal targeted for either the first or second memory device, and wherein the first memory device or second memory device is selectively decoupled from the bus in response to a change in state in the address signal.

22. The state decoder circuit of Claim 21, wherein the address signal comprises a row address strobe signal.

23. The state decoder circuit of Claim 21, wherein the address signal comprises a column address strobe signal.

24. A electronic device comprising:

a printed circuit board;

a memory controller mounted on said printed circuit board;

a bus switch mounted on said printed circuit board;

a first data bus connecting said memory controller and said bus switch;

a state decoder configured to receive an address signal targeted for either the first or second memory device, and wherein the first memory device or second memory device is selectively decoupled from the bus in response to a change in state in the address signal;

a plurality of memory devices including at least a first and a second memory device mounted on said printed circuit board; and

a second data bus connecting said bus switch to said first memory device and a third data bus connecting said bus switch to said second memory device, wherein said bus switch is configured to couple said first data bus to said second data bus during memory accesses directed to said first memory device, and wherein said bus switch is configured to couple said first data bus to said third data bus during memory accesses directed to said second memory device.

25. The state decoder circuit of Claim 24, wherein the address signal comprises a row address strobe signal.

26. The state decoder circuit of Claim 24, wherein the address signal comprises a column address strobe signal.

27. A electronic device comprising:

a printed circuit board;

a memory controller mounted on said printed circuit board;

a bus switch mounted on said printed circuit board;

a first data bus connecting said memory controller and said bus switch;

a state decoder configured to receive an address signal targeted for either the first or second memory device, and wherein the first memory device or second memory device is selectively decoupled from the bus in response to a change in state in the address signal;

a plurality of memory devices including at least a first and a second synchronous-DRAM memory device mounted on said printed circuit board; and

a second data bus connecting said bus switch to said first synchronous-DRAM memory device and a third data bus connecting said bus switch to said second synchronous-DRAM memory device, wherein said bus switch is configured to couple said first data bus to said second data bus during memory accesses directed to said first memory device, and wherein said bus switch is configured to couple said first data bus to said third data bus during memory accesses directed to said second memory device.

28. The state decoder circuit of Claim 27, wherein the address signal comprises a row address strobe signal.

29. The state decoder circuit of Claim 27, wherein the address signal comprises a column address strobe signal.